Interval Type-II Fuzzy Logic Control of Neutral DC Compensation Method to Moderate DC bias in Power Transformer

Olanrewaju A. Lasabi, Andrew G. Swanson, and Alan L. Jarvis

***Abstract*—Direct current flow through power transformers in HVDC systems can lead to significant half-cycle saturation issues, putting the power system at risk. The HVDC system can function in monopolar ground return and unbalanced bipolar without earth return conductors. During these two HVDC modes of operation, a substantial direct current flows through the HVDC ground terminals, creating a ground DC potential difference between the neutrally grounded transformers. As a result, DC flows through the neutrals into the transformer windings. The study presents a transformer-neutral DC compensating device incorporating a novel control to solve the issue. Using a proper control strategy, injecting reverse DC into the grounding grid can compensate for direct current flow in transformer windings to mitigate the biased operating flux of power transformers. In this article, an in-depth analysis of transformer response to DC bias was investigated. Then, an Interval type-II fuzzy logic control (IT2FLC) was proposed as an effective control strategy for managing the neutral DC compensating system. Its robustness was assessed and analysed by comparing it with type-I fuzzy logic-based (T1FLC) and a PI-based compensation system. The control performance is examined using MATLAB/Simulink models and validated with rapid control prototype tests conducted with a Speedgoat™ real-time target machine, assessing the transient response, oscillations, and settling time of the compensation device under DC bias voltage variations. The outcomes indicate that the IT2FLC controls the compensation device more effectively than other controllers to mitigate half-cycle saturation. This approach introduces a novel strategy to prevent transformer half-cycle saturation.**

***Index Terms*—power transformers, DC bias, fuzzy logic control, high-voltage direct current transmission, neutral compensation method,**

I. Introduction

THE utilisation of high voltage direct current (HVDC) transmission lines is steadily expanding, driven by their capability to transmit large amounts of power over long distances with greater efficiency. In addition, the emergence of high-capacity semiconductor devices together and in cooperation with the new technologies for developing more efficient power converters has also led to the increasing use of HVDC [1]. HVDC systems can operate in two distinct configurations. The first is an unbalanced bipolar system, where two conductors of opposite polarity are used, and the system is designed without the need for a ground return conductor. Alternatively, HVDC systems can function as a monopolar system that uses a single conductor and relies on the earth as a return path, a method known as ground return mode.

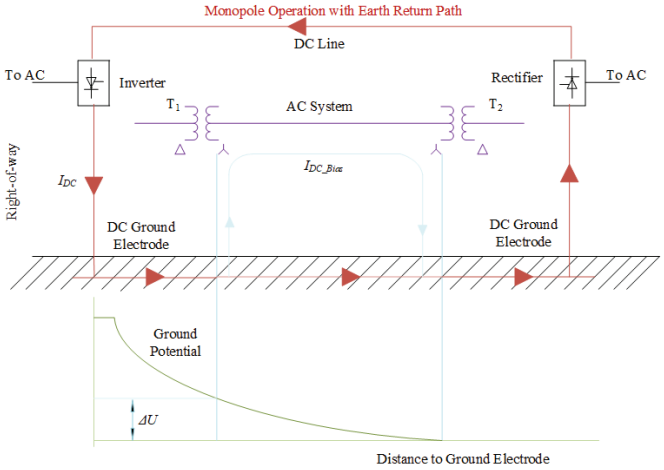

Fig. 1. Monopole operation of HVDC with ground return in an AC network Showing Ground Potential Distribution [1].

The use of a ground return conductor can be decided based on technical, economic and environmental factors [1]. In both operational modes of an HVDC system, a substantial amount of direct current is directed through HVDC ground electrodes into the earth. This flow of DC can create an earth surface potential difference, particularly between the neutral points of grounded transformers or between transformers within nearby AC systems [2]-[3]. This is illustrated in Fig. 1, representing an HVDC monopolar system with a ground return path. A similar event occurs during a geomagnetic disruption, also known as geomagnetically induced currents (GIC), whereby an intense solar wind can interact with the earth's geo-electric field and

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cause potential differences [4].

The flow of DC through the transformer windings drives the power transformer into half-cycle saturation [1]-[3], [5], which poses a significant risk to the safe and economic operations of the whole power grid. Saturation of a power transformer can result in several negative consequences. These may include vibration and audible noise [5], as well as excessive heating and hotspots in power transformers [6]. These effects can compromise the transformer's efficiency and longevity, potentially leading to transformer breakdown. The distorted magnetisation current leads to a severe loss of reactive power [7], and the harmonic component in the current interacts with protective relay devices, transformers, shunt capacitors and static var compensators (SVCs) on the power system [8]-[9]. Hence, preventive measures are critical to protect power equipment and efficient power systems operations.

In a bid to mitigate half-cycle saturation in power transformers, several mitigating strategies have been implemented. The first technique is the insertion of neutral blocking devices (NBDs) between the ground and the neutrals of the power transformer. A type of NBD, which utilises a large power capacitor to break off the flow of neutral DC along the conducting path, was implemented in [10]. In [11], an auxiliary bypass and airgap were connected in parallel to a large capacitor to create a conducting path for fault current during fault. To achieve higher reliability and improve the economic and technical performance of NBDs, a large power capacitor safeguarded by a metal oxide varistor (MOV) with an auxiliary bypass was implemented in [12] to curtail DC flow in transformer neutrals. During GIC disturbances, a bucking motor was also proposed for blocking the flow of DC in [13]. A large capacitor connected in parallel with a resistor was implemented without a bypass device in [14] to reduce DC flow in power transformer neutrals. The zero-sequence impedance varies significantly due to the enormous power capacitors used in the transformer neutrals for restraining DC flow. This capacitor type of NBD negatively influences real-time contingency, neutral overvoltage, ferroresonance, oscillation and relay settings [1]-[2].

Another type of NBD was also proposed in [4], where semiconductors were utilised as switching devices to limit DC flow in transformer neutrals through pulse width signals. The control and protection strategies of this type of NBD are complex. Due to the inability of NBDs to mitigate the flow of DC in an autotransformer with series windings, series compensations were proposed in [15] to cut off the flow of DC on transmission lines. Series compensation is not economically suitable to curtail half-cycle saturation due to the enormous cost and size involved.

In [16], another type of NBD that involves utilising a resistor was implemented. The resistor was connected in parallel with a spark gap. Neutral DC flow will reduce with a higher impedance resistor placed in series with the transformer neutral point. Though the approach was categorised as inexpensive in restraining neutral DC flow, it has drawbacks: DC bias can only be reduced and not eliminated [1], [16]. The resistance of the resistor also varies with different transformers in different locations; the resistor needs to be calibrated based on the magnitude of DC for individual transformer locations [1]. A higher value of this resistance will not only affect protective relay settings negatively, but it could also result in an ineffective connection between transformer neutrals point and ground, leading to overvoltage during system fault [2].

Various methods of restraining DC flow in power transformers have also been proposed. In [17], by utilising a finite element model built for a single-phase power transformer, the authors modelled an auxiliary winding with a controllable DC source to limit half-cycle saturation. A grounding grid with a very high resistance was also suggested and implemented for power transformers to reduce neutral DC flow in [18]. The drawbacks of these methods are apparent. The auxiliary winding method has yet to be utilised due to its additional vigorous design of power transformers and the implementation of complex measurement and control systems. Safety problems and overvoltage issues occur in transformer neutrals due to the high resistance of the grounding grid.

This research proposes a novel approach to impede transformer half-cycle saturation through modelling and simulation on MATLAB/Simulink. It utilises a neutral direct current compensation method to indirectly recompense the direct magnetomotive force (MMF) in power transformers, thereby alleviating transformer half-cycle saturation issues in HVDC systems. This compensation method will indirectly produce a supplementary direct MMF component that counteracts the MMF induced by the DC flowing within the power transformer. By doing so, it effectively neutralizes the magnetic effects caused by the DC, thereby maintaining the transformer's core within its normal operational condition and preventing saturation. Compared with NBDs, this compensation method does not alter the insulation configuration of the transformer neutral, protective relay configurations and system contingencies [1]-[2], [8]. This method can also work for different transformers simultaneously, making it more economical. It is safe and reliable for the power transformer and around the substation.

Based on the various assessments from previous studies, this compensation method faces challenges such as inaccurate determination of the injected current magnitude in real-time, leading to less compensation and over-compensation issues. In [2], the authors manually adjusted the voltage source to counteract DC bias effects. In [8], the authors recommended implementing a proportional-integral (PI) controller to regulate the voltage source within the compensating device. The controller operates effectively only within a designated range of conditions. When there is a change in the operating range, it becomes necessary to recalibrate the controller’s gains to ensure continued optimal performance. A trial-and-error process conventionally tunes the gains, and the result depends on the engineer's intuition or expertise. Hence, the conventional PI control performance needs to be improved and up to the required level for nonlinear and dead time processes. It is important to highlight that this study builds upon the work presented in [19]. The newly proposed method offers enhanced performance consistency compared to the approach outlined in

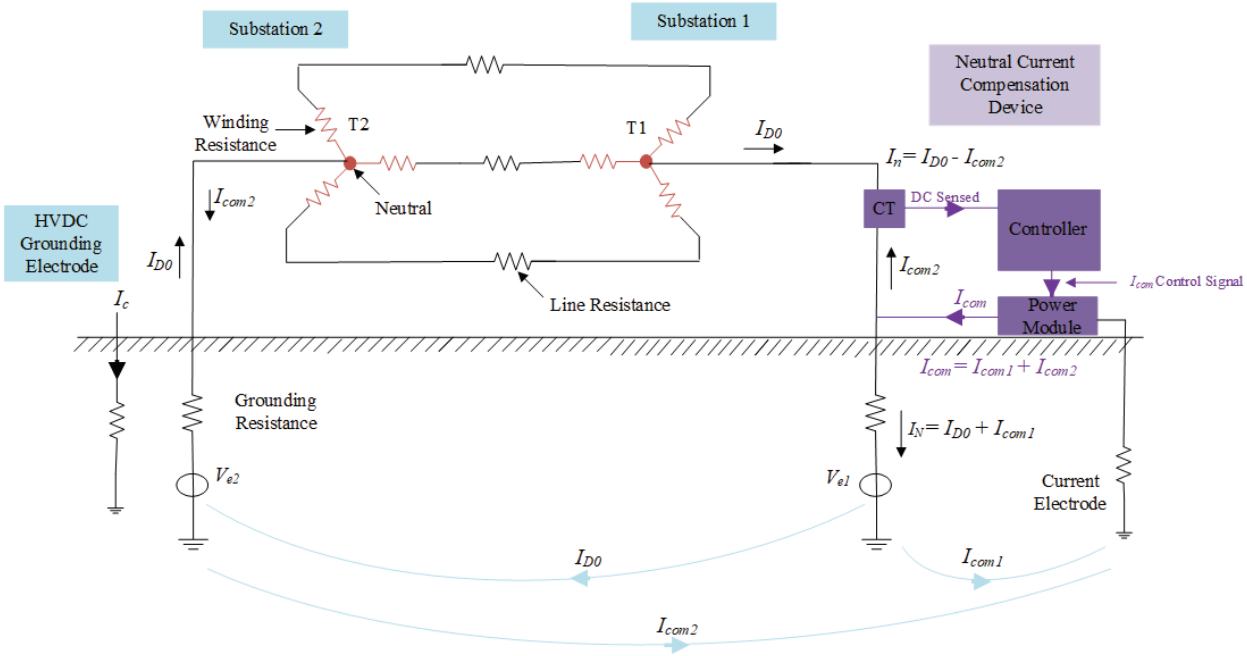

Fig. 2. Illustration of the compensation device at work in a power system. I_{com} depicts the power module output current; I_n is the neutral current after the compensation device is used; I_{D0} is the neutral current before the compensation device is used [8], [19].

[19], demonstrating significant improvements in reliability and effectiveness. Therefore, this research proposes developing a closed-loop controller based on an Interval Type-II Fuzzy Logic Controller (IT2FLC) for efficient and effective real-time dynamic compensation of neutral DC flow in power transformers. The IT2FLC was compared with PI and Type-1 Fuzzy Logic Controller (T1FLC) to demonstrate its robustness. To date, no other information about this controller is available.

II. Theoretical Solution

The mechanism of half-cycle saturation of power transformer caused by induced DC flow in HVDC systems has been discussed extensively in [1], [3], [4], [8]. Therefore, this research presents a DC compensation method with a novel controller based on a fuzzy inference system to curb transformer half-cycle saturations. The core concepts of this method are demonstrated in Fig. 2. During the monopolar activity of HVDC, the grounding electrode of the HVDC injects a direct current (I_c). This I_c induces a ground potential increase. In the power grid containing the grounded transformers and transmission lines, as described in Fig. 2, the ground potential rise of substation one and substation two are significantly different, which results in a potential difference (V_{e2} - V_{e1}). A DC circulates through the above-ground power grid and ground, a DC circulates between substation one and substation two, resulting in the transformer's half-cycle saturation. The DC compensating method consists of a controllable power module linked to the transformer's neutral point. This module delivers into the grounding grid, a compensation current I_{com}, to reduce the transformer's neutral DC in substation one from I_{D0} to I_n [8].

$$I_n = I_{D0} - I_{com2} \tag{1}$$

$$I_{com2} = -I_{com1} + I_{com} \tag{2}$$

It is evident that by modifying the injected current I_{com}, the direct current flowing through the transformer neutral can be subdued to a level below a predetermined benchmark, I_{lim}, for neutral DC. It can be seen from the mechanism of the compensation method that for a fixed value of I_c, direct current movement within the system is influenced by ground potential rise (GPR). The actions of the substation earth grid, compensating device current electrode coupled with the grounding electrodes of the transmission system create this GPR. Grounding models are required in other to model GPR. GPR can be computed efficiently for some inhomogeneous ground models (Cylindrical [20], hemispheroidal [21], stratified [22] and spherical [23]). Using complex image method, ground potential coupling matrices can be calculated for layered or homogeneous earth [2], [24],. Evaluating the effectiveness of the mechanism of DC compensation method involves electric field and circuital analysis. Hence from Fig. 2, the nodal potential mathematical expressions for the AC system are derived as [24]:

$$YV_e = I \tag{3}$$

$$I = AP + I_{com} \tag{4}$$

$$P = M_G I_N - M_c I_{com} + M_{dc} I_c \tag{5}$$

$$I_N = A(V_e - P) \tag{6}$$

where I_c and I_N depict the DC infused into the HVDC earth terminal and substation earth grid, respectively. M_c represents

the mutual resistance matrix between the current terminal (auxiliary earth terminal) and all substations. M_{dc} also depicts the mutual resistance matrix between the HVDC earth terminals and all the substations. M_G represents the matrix of mutual resistances between all the earth grid nodes at the substations. I_{com} and P denote the compensating device nodal-infused current and nodal substation GPR. For all substations, A represents the matrix of earth conductance at the nodes. I and V_e denote the infused nodal current and voltage vector, respectively. Y depicts the nodal admittance matrix. As expressed in (3) to (6), the nodal potential distribution of the system is formulated as [2], [24]:

$$V_e = ZM_{dc} - ZM_cI_{com} + Y^{-1}I_{com} \quad (7)$$

$$Z = [(E + M_GA)A^{-1}Y + M_GA]^{-1} \quad (8)$$

where E and Z denote the identity matrix and field-circuit coupling matrix. In our previous study [19], we provided a detailed explanation of the operational mechanism through which the compensation method effectively removes neutral DC. This is achieved by selecting the appropriate compensating current, I_{com}, to eliminate the unwanted DC components. Therefore, a DC compensation device based on the compensation method can be developed. Generally, the compensation device can be regarded as an active filter designed to address the direct current flow within the neutral lines of a transmission system. The device is installed at the transformer neutral point, as seen in Fig. 2, to counteract the direct current before it enters the transformer windings via the neutrals. This strategic placement ensures that the DC is effectively managed prior to impacting the transformer components. The compensation device is primarily composed of three key modules: the controllable power module, the control and measuring system [19]. This research focuses on the control system: building a robust closed-loop IT2FLC to control the compensation device.

III. System Modelling

A comprehensive description of the system model used in this research is provided in our earlier study [19] and is depicted in Fig. 3. The model utilizes a 200 MW HVDC transmission system, rated at 800 A and 250 kV, and was created by utilizing MATLAB/Simulink software. In other to inject direct current bias into the windings, a variable DC voltage source is linked, via the star-connection side, to the neutral point of the transformer. This DC bias voltage was adjusted to 0V, 300V, and 400V to examine how different levels of DC bias influence the power transformer.

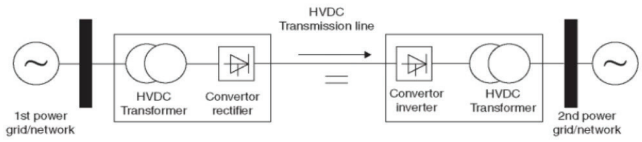

Fig. 3. HVDC Model.

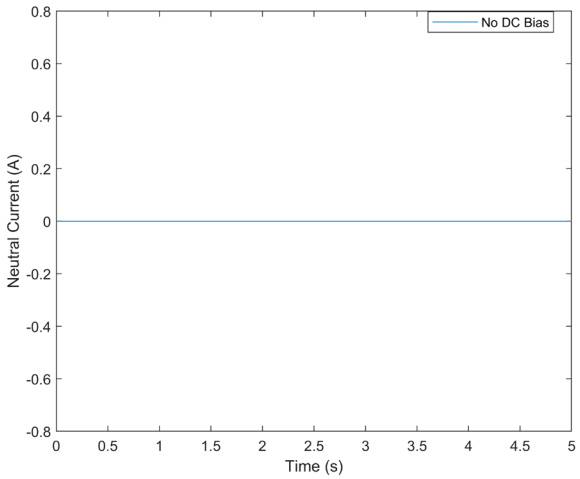

Fig. 4. Transformer neutral current in the absence of DC bias.

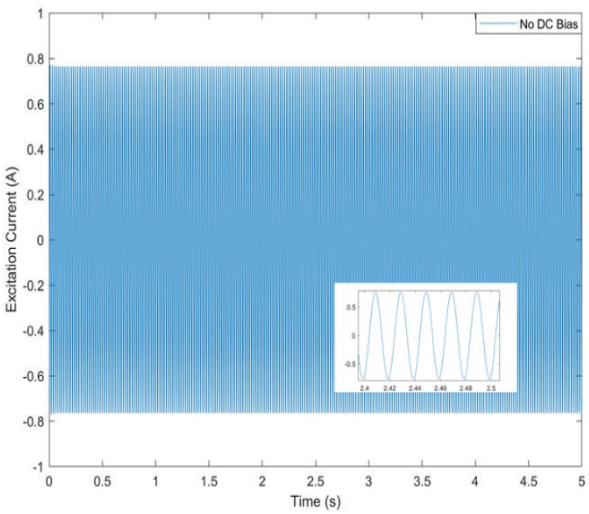

Fig. 5. Transformer excitation current in the absence of DC bias

A. Analysis of Excitation and Neutral Current under Varying DC Bias Conditions.

The authors in [3] defined the relationship that exists between permissible DC and rated current. For single-phase power transformers, 0.3% of the rated current was specified as the allowable direct current. In the case of three-phase transformers, 0.5% of rated current was defined for five-limb while 0.7% of rated current was specified for three-limb. In this article, the permissible DC for single-phase transformers has been selected as 10A. As depicted in Fig. 3, the controllable DC voltage source coupled with an earth resistance of 5Ω was utilised in the simulation to infuse direct current through the windings at 0.5s and varied at different levels to examine the impact of DC bias: 0V, 300V and 400V. The neutral current measured is presented in Fig. 4, Fig. 6 and Fig. 8.

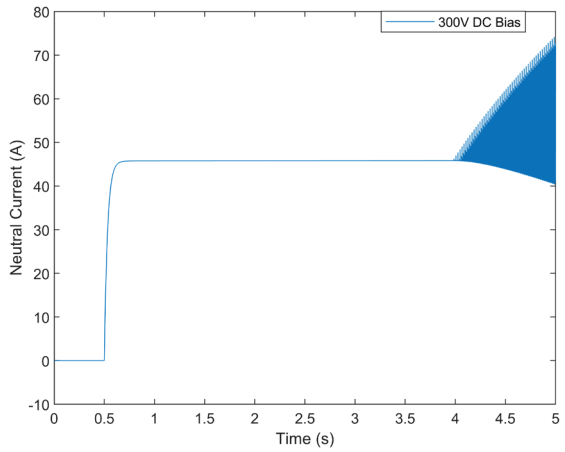

Fig. 6. Transformer neutral current with 300V DC bias.

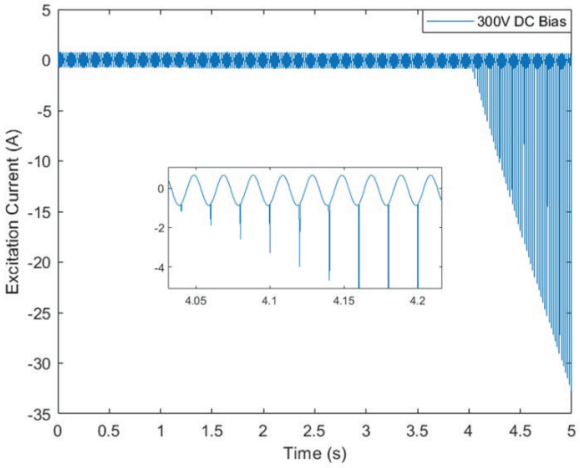

Fig. 7. Transformer excitation current with 300V DC bias.

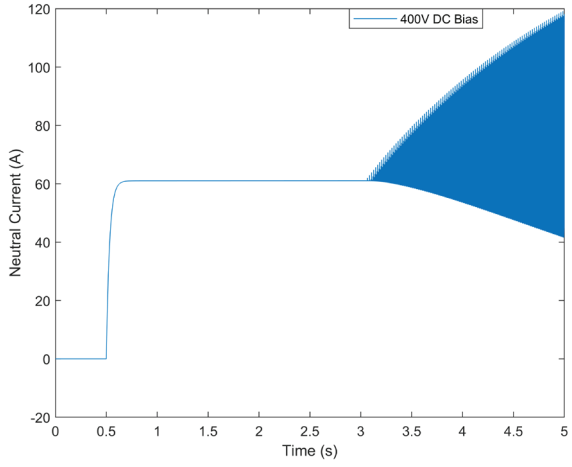

Fig. 8. Transformer neutral current with 400V DC bias.

It can be deduced that as this DC in the neutral increases, the direct current flowing through the windings also increases, affecting the excitation current (a combination of the magnetisation current and core loss current). The excitation current waveform of phase A was monitored. As shown in Fig. 5, Fig. 7 and Fig. 9, the excitation current gets distorted, and the distortion becomes severe as the level of DC increases. The waveform becomes peaky in the negative half-cycle and becomes evident with increasing amplitude as DC increases. Also, as the DC level increases, the waveform of the positive half-cycle becomes progressively flattened, with its peak amplitude diminishing and approaching zero. This flattening effect indicates a significant distortion of the waveform caused by the rising DC bias.

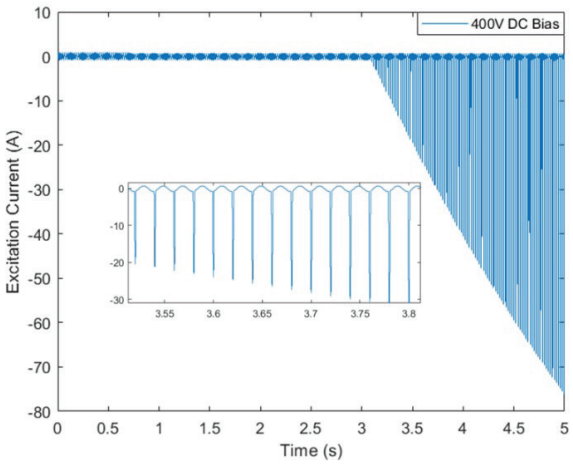

Fig. 9. Transformer excitation current with 400V DC bias.

IV. Proposed Approach

This section presents the direct current compensating device equipped with the newly introduced fuzzy control. The device introduces a counteracting direct current bias through the transformer neutral to neutralize the existing direct current bias. The focus of this research is the control system, which is discussed in detail in this section.

A. Power Module

The power unit consists of a controllable DC voltage source that generates the required direct current needed to counteract the neutral direct current. Both boost and buck-boost converters were utilised. The voltage output of boost DC-DC converters is of a similar polarity as the input voltage and can produce a voltage more significant than the input voltage. Hence, it produces a positive DC voltage when required by the compensation device. Furthermore, the voltage output of buck-boost converters is of opposite polarity to that of the input voltage and generates a voltage less than or greater than the input voltage. This inverting characteristic of the buck-boost converter makes generating a negative DC voltage worthwhile when required by the compensation device. The schematics are shown in Fig. 10 and Fig. 11. The parameters utilised for the design of the converters were calculated for operations in continuous conduction mode. Allowing 5% current ripples, the conventional formulas in (9) to (14) [25] were used to obtain the minimum values of capacitors and inductors required for the converters to function in continuous conduction mode. These values can be increased to reduce ripples. Table I presents the parameters utilized for the design of the converters.

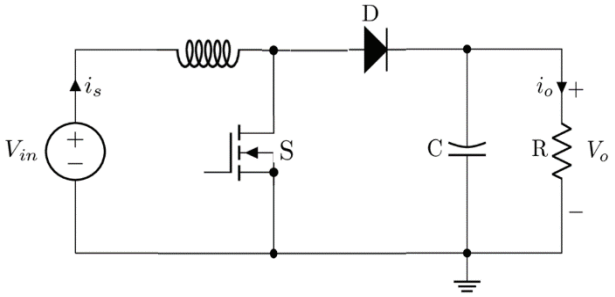

Fig. 10. Boost DC-DC converter.

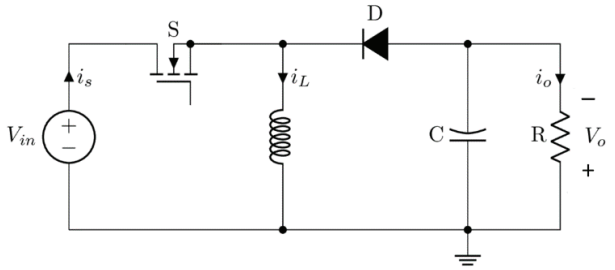

Fig. 11. Buck-Boost DC-DC converter.

TABLE I
CIRCUIT PARAMETERS FOR DC-DC CONVERTER

Parameters	Boost	Buck-Boost
Inductance (L)	0.44 mH	0.64 mH
Capacitance (C)	5090 µF	8440 µF
Load Resistance	5 Ω	5 Ω
Input Voltage	48 V	250 V
Output Voltage	600 V	600 V
Switching freq.	10 kHz	10 kHz

Boost Converter:

$$L = \frac{D(1-D)R}{2f_s} \tag{9}$$

$$D = 1 - \frac{V_{in}}{V_{out}} \tag{10}$$

$$C = \frac{D}{2f_s R} \tag{11}$$

Buck-Boost Converter:

$$L = \frac{(1-D)R}{2f_s} \tag{12}$$

$$C = \frac{D}{2f_s R} \tag{13}$$

$$D = \frac{V_{out}}{V_{out}-V_{in}} \tag{14}$$

where D, R, f_s, V_{out} and V_{in} are the duty cycle, load resistance, pulse width modulation (PWM) switching frequency, output voltage and input voltage, respectively.

B. DC Bias Compensation Device Control Techniques

The direct current compensating device is capable of employing closed-loop control algorithms to accomplish its aims, particularly in terms of dynamic performance. The duty cycle rate controls the voltage output of the converter. Due to its simplicity, the voltage mode control strategy is utilised in this study to control the converters. Pulse width modulation (PWM) generator and a voltage loop are generally utilised in this technique. This voltage loop uses the converter's output voltage error and the change in error to produce the reference waveform for the PWM generator [25]. In this study, IT2FLC, T1FLC and PI controls are utilised in the neutral direct current compensating device to replace the voltage loop. Contrasting the reference waveform signal acquired from the controller's output with the carrier waveform, the PWM generator generates the required signal needed for switching. The PI control configuration for the device has been detailed in [19].

1) T1FLC in Neutral DC Compensation Device

The schematic of the T1FLC used to control the compensation device is shown in Fig. 12. Fuzzifier, rule base, inference engine and defuzzifier are the four components of T1FLC. All input data passing through the first fuzzification stage in the T1FLC are categorised into appropriate linguistic values or sets. In the inference engine, a fuzzy control operation is generated based on the knowledge of a set of controller rules and the linguistic variable definition. In the defuzzifier section, the inferred fuzzy outputs are converted into crisp outputs [26].

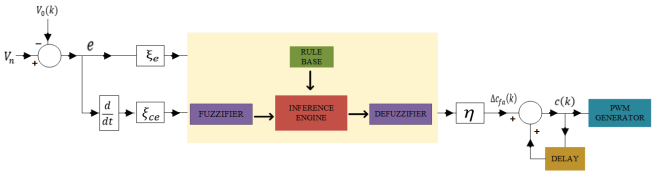

Fig. 12. Schematics of T1FLC

The fuzzy control output is the variations in the waveform of the reference signal, which ultimately defines the variations in the duty cycle. This reference waveform, $c(k)$, can be obtained by the summation of the waveform of the previous reference, $c(k-1)$, with the change in reference waveform calculated, $\Delta c\,(k)$. This can be expressed as:

$$c(k) = c(k-1) + \eta * \Delta c_{fa}(k) \tag{15}$$

where η is the gain of the controller. This expression in (15) depicts an integrating process that reduces the controlled system's steady-state error. The calculated waveform of the reference signal, which is also the duty cycle, $c(k)$, constitutes the input through the PWM generator. The T1FLC designed for the compensation device, as shown in Fig. 12, comprises one output and two inputs. These two inputs are the change in voltage error, $\Delta e(k)$, and the voltage error, $e(k)$, at a k^{th} moment. The output is the change in the duty cycle, $\Delta c_{fa}(k)$, at the k^{th} instant. The two inputs can be obtained by:

$$e(k) = V_n - V_0(k) \tag{16}$$

$$\Delta e(k) = e(k) - e(k-1) \tag{17}$$

where *e(k-1)* depicts the voltage error at *(k-1)th* sampling moment, and $V_o(k)$ represents the voltage output of the converter at the k^{th} moment. V_n is the voltage signal of the DC bias sensed within the neutral; it is initially zero until the DC bias exceeds 10A, which is the allowable DC for single-phase transformers used in this article, as explained earlier. This 10A acts as the threshold; the output of the neutral DC compensating device, which represents the output voltage of the converter, will be zero (remain off) until this threshold is reached. The gains ξ_e, ξ_{ce}, and η are tuned by using an artificial bee colony optimisation algorithm described in [27] to obtain a preferred output.

As depicted in Fig. 13, the universe of the voltage error, *e*, change in duty cycle, Δc_{fa} , and change in voltage error, Δe, are split into five fuzzy sets (FS). Triangular membership functions (MFs) were utilised for the FS, for both the output and input MFs, owing to their application efficiency and simplicity. Each MF of the fuzzy variable is allotted to an abbreviated linguistic label: PB (Positive Big), PS (Positive Small), ZE(Zero), NS (Negative Small), and NB (Negative Big). The input and output membership values were normalised in the range (-1,1) using appropriate scale factors.

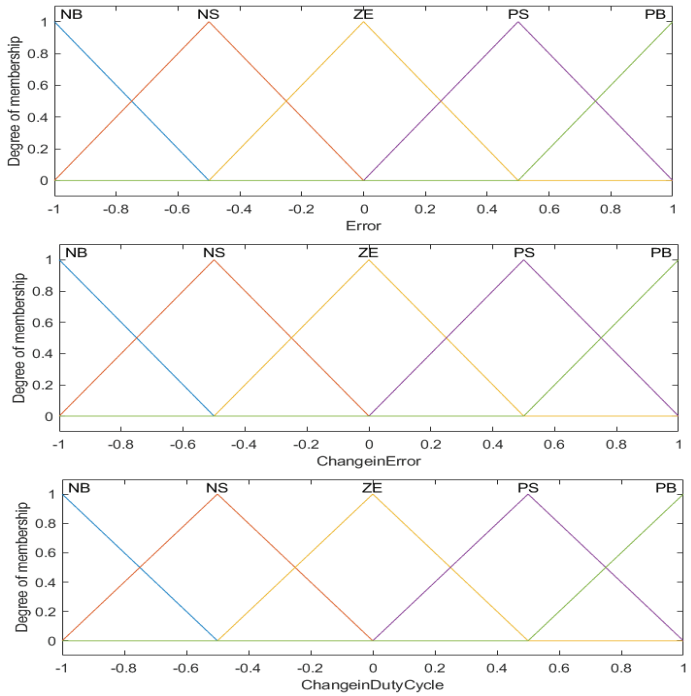

Fig. 13. T1FLC Membership Function.

The control rules for T1FLC in this study were derived from analysing the system dynamics. The voltage output of the converter is mathematically related to both the duty cycle and the input voltage, as expressed in (10) for boost and (13) for buck-boost. A general approach can be extracted for the two converters by analysing these two equations: the duty cycle of any of the converters must be increased to increase the magnitude of the converter output voltage. This conclusion forms the basis for designing the control rules for fuzzy controllers and will be the same for both converters utilised in this study.

TABLE II
NEUTRAL DC COMPENSATION DEVICE FUZZY RULES

		$e(k)$				
		NB	NS	ZE	PS	PB
$\Delta e(k)$	NB	PB	PB	PS	ZE	NS
	NS	PB	PS	PS	NS	NS
	ZE	PS	PS	ZE	NS	NS
	PS	PS	PS	NS	NS	NB
	PB	PS	ZE	NS	NB	NB

More detailed fuzzy control rules are formed, as shown in Table II. These rules are twenty-five, and they depict the relationship being established between the fuzzy control inputs and output. Each fuzzy rule is structured in the following format:

$$R^i\text{: IF } e \text{ is } H_e^i \text{ AND } \Delta e \text{ is } H_{\Delta e}^i \text{ THEN } \Delta c_{fa} \text{ is } J^i$$

where H_e^i and $H_{\Delta e}^i$ are the FSs denoting the i^{th} antecedent pairs and J^i representing the i^{th} consequent in their respective universe of discourse. As depicted in Table II, a particular union of the rate of change in voltage error, $\Delta e(k)$ and voltage error, *e(k),* is equivalent to a specific change in duty cycle. For instance, IF *e* (voltage error) is NS AND Δe (change in voltage error) is PB, THEN it is equivalent to ZE Δc_{fa} (change in duty cycle).

Once the control rules associated with the input values have been selected, the fuzzy inference technique is applied to compute the outcome of each rule. The operation of a defuzzifier, using the centroid method, is required as the last step to retrieve the crisp output from the inferred outcome. This can be expressed as:

$$\Delta c_{fa} = \frac{\sum_{i=1}^{N} Y^i * J^i}{\sum_{i=1}^{N} Y^i} \tag{18}$$

where Y^i is the firing weight of each rule. Once the design of the T1FLC is achieved, the membership values dictate the performance of the system. This performance might not be exact to the preferred. Changing the membership function under any condition to achieve the preferred output and accuracy is a complicated process but gains (ξ_e, ξ_{ce}, and η) can be employed. By varying these gains, the membership values can easily be altered to improve the system's overall performance.

2) IT2FLC in Neutral DC Compensation Device

The schematics of the IT2FLC used to control the compensation device is shown in Fig. 14. Fuzzifier, rule base, inference engine, type-reducer and defuzzifier are the five components of this controller. IT2FLC FSs are utilized to fuzzify the input variables, change in voltage error (Δe) and voltage error (*e*), due to their simplicity and evenly distributed uncertainties between all permissible primary memberships. These FSs actuate the inference engine and the rule base to

bring about output FSs of type-II. In contrast to T1FLC, before proceeding with the defuzzification process to obtain crisp outputs, the inferred outputs from the inference engine must be type-reduced [26], [28].

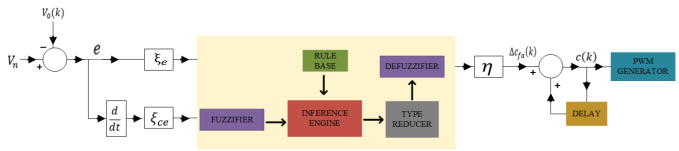

Fig. 14. Schematics of IT2FLC

Triangular MFs were used for the inputs and output of the interval type-II (IT2) FSs. The footprint of uncertainty (FOU) is used to establish the uncertainty boundary in the IT2 fuzzy set membership functions due to the uncertainty connected with the type-1 fuzzy set. As shown in Fig. 15, the upper membership function (UMF) is the FOU's outside boundary, whereas the lower membership function (LMF) is its inner boundary.

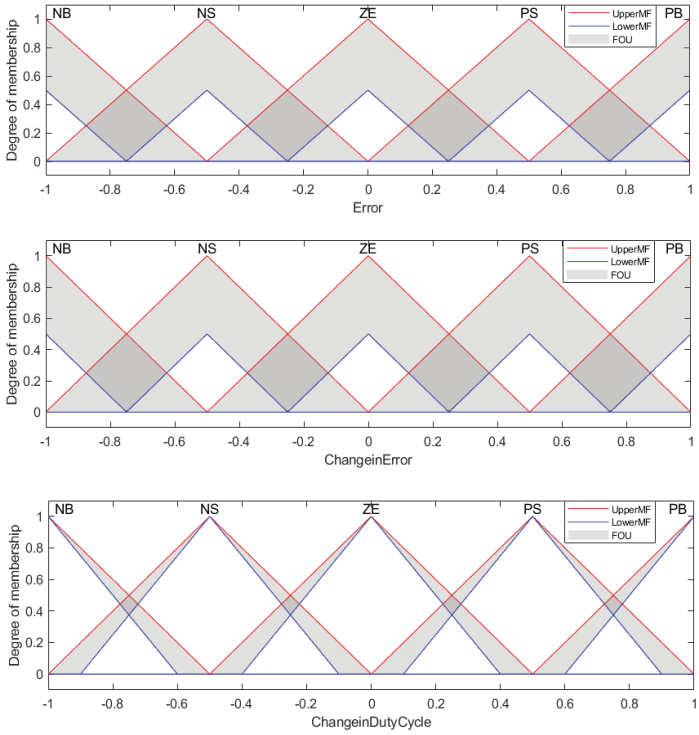

Fig. 15. IT2FLC Membership Function.

In IT2FLC, the rule structure remains the same as that of T1FLC but the consequents and antecedents are depicted by IT2 FSs, and are is expressed as:

$$R^i\text{: IF } e \text{ is } \tilde{H}_e^i \text{ AND } \Delta e \text{ is } \tilde{H}_{\Delta e}^i \text{ THEN } \Delta c_{fa} \text{ is } [J_l^i, J_r^i]$$

where $\tilde{H}_e^i$ and $\tilde{H}_{\Delta e}^i$ are the IT2 fuzzy sets of the antecedent part, which defines both input variables. $[J_l^i, J_r^i]$ represents the weighting interval set in the consequent part. In combination with the fired rules, the inference engine produces a mapping from input IT2FLC FS to output IT2FLC FS. The Meet operation is utilized in the inference engine to connect the antecedents in the rules. Also, by utilizing the extended sup-star composition, the membership grades in the input sets are joined with those in the output sets, and Join operation is utilized to combine multiple rules. As in the T1FLC system, the firing strength of the IT2FLC can be derived through the inference process:

$$P^i = [\overline{p}^i, \underline{p}^i] \tag{19}$$

where $\overline{p}^i$ and $\underline{p}^i$ can be expressed as:

$$\overline{p}^i = \overline{\mu}_{\tilde{H}_e^i}(e) * \overline{\mu}_{\tilde{H}_{\Delta e}^i}(\Delta e) \tag{20}$$

$$\underline{p}^i = \underline{\mu}_{\tilde{H}_e^i}(e) * \underline{\mu}_{\tilde{H}_{\Delta e}^i}(\Delta e) \tag{21}$$

where $\overline{\mu}$ and $\underline{\mu}$ represents the lower and upper membership grade respectively. By utilizing the center-of-set method, the type-reduced set is derived as [26], [28]:

$$\Delta c_{cos} = \int_{j^1 \in [j_l^1, j_u^1]} \cdots \int_{j^M \in [j_l^M, j_u^M]} \int_{p^1 \in [\overline{p}^1, \underline{p}^1]} \cdots \int_{p^M \in [\overline{p}^M, \underline{p}^M]} 1 \Big/ \frac{\sum_{i=1}^M p^i . j^i}{\sum_{i=1}^M p^i} = [\Delta c_l, \Delta c_r] \tag{22}$$

where Δc_{cos} represents an interval type1 fuzzy set deduced by the leftmost and rightmost points (Δc_l and Δc_r respectively). Utilizing the consequent centroid set $[j_l^i, j_r^i]$ and the firing strength $p^i \in P^i = [\underline{p}^i, \overline{p}^i]$ (i=1,…,*M*), Δc_l and Δc_r can be expressed as follows:

$$\Delta c_l = \frac{\sum_{i=1}^M p_l^i . j_l^i}{\sum_{i=1}^M p_l^i} \tag{23}$$

and

$$\Delta c_r = \frac{\sum_{i=1}^M p_r^i . j_r^i}{\sum_{i=1}^M p_r^i} \tag{24}$$

Finally, the average of Δc_l and Δc_r is the defuzzified crisp output (change in duty cycle) that will be obtained from IT2FLC. This can be expressed as:

$$\Delta c_{fa} = \frac{\Delta c_l + \Delta c_r}{2} \tag{25}$$

Δc_{fa} is then used in (15) to obtain the calculated duty cycle signal, which will be sent to the PWM generator to generate an appropriate switching waveform for the DC converters.

V. Simulation Results and Discussions

To analyse the impact of the newly introduced IT2FLC on the capabilities of the compensating device, the neutral DC direct current compensating was tested using three different controllers: IT2FLC, T1FLC, and PI. Their design techniques have been described in the section above. As explained in the previous section, two converters: buck-boost and boost converters, were utilised in the compensating device. The compensation device is designed to allow only one converter to operate at any given time, depending on the DC bias polarity detected in the neutral. This ensures the appropriate converter is activated based on the sensed DC bias. Hence, to assess the

effectiveness of the IT2FLC being proposed, simulations were conducted under two distinct direct current bias scenarios: one with a negative and the other with a positive DC bias. In each scenario, four distinct levels of direct current bias voltage—200V, 300V, 400V, and 600V—were introduced at 0.5 s.

A. Scenario One: Positive DC Bias

The simulation results of the three controllers under different positive direct current bias voltages are presented in this section. It should be noted that the buck-boost converter was enabled in the compensation device during these operations. Fig. 16, depicting the results for a +200V direct current bias voltage, shows that the PI control required 0.58 s to eliminate the bias and achieved a total settling time of 1.08 s. T1FLC eliminated the bias in 0.21 s, achieving a settling time of 0.71 s, whereas IT2FLC removed the direct current bias in 0.07 s and had a settling time of 0.57 s.

In the case of the +300V direct current bias voltage, Fig. 17 demonstrates that the PI control eliminated the bias in 0.54 s, achieving a settling time of 1.04 s. T1FLC removed the bias in 0.12 s, with a settling time of 0.62 s. IT2FLC, on the other hand, achieved direct current bias cancellation in just 0.05 s and had a settling time of 0.55 s.

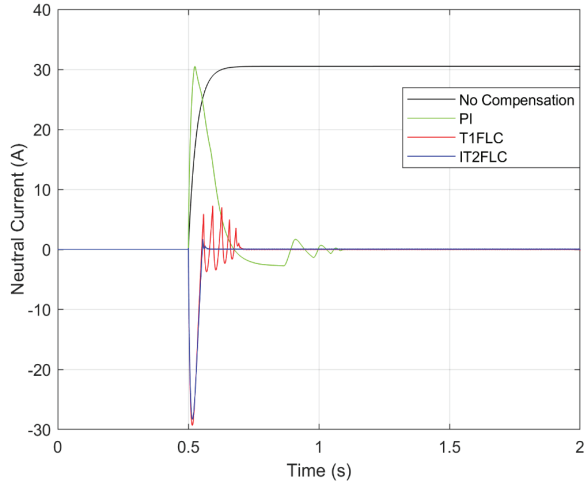

Fig. 16. Neutral current for positive 200V DC bias infused at 0.5s.

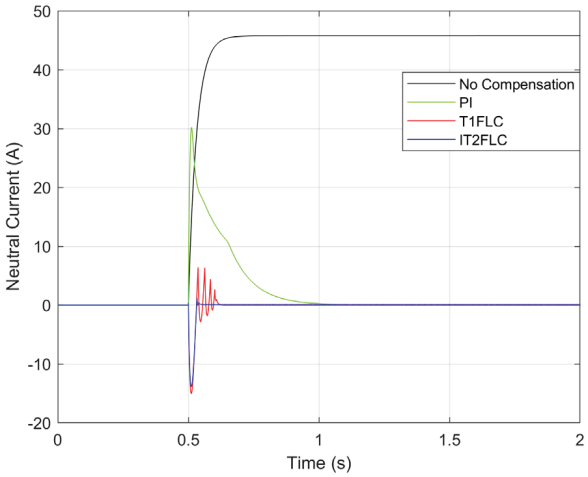

Fig. 17. Neutral current for positive 300V DC bias infused at 0.5s.

Additionally, Fig. 18, which presents the results for the +400V bias voltage, reveals that the PI control required 0.59 s to eliminate the bias, with a settling time of 1.09 s. T1FLC neutralised the bias within 0.05s, with a settling time of 0.55 s, while IT2FLC neutralised the bias in 0.03 s with a settling time of 0.53 s. Also, in the case of the +600V direct current bias voltage, Fig. 19 indicates that the PI control eliminated the bias in 0.64 s, achieving a settling time of 1.14 s. The bias was also eliminated with the use of T1FLC in 0.03 s, obtaining a settling time of 0.53 s, and IT2FLC eliminated the bias in 0.01s while attaining a settling time of 0.51s. As anticipated, the proposed IT2FLC performed better, having the least current deep with no oscillations compared to T1FLC coupled with enhanced transient responses when juxtaposed with T1FLC and PI.

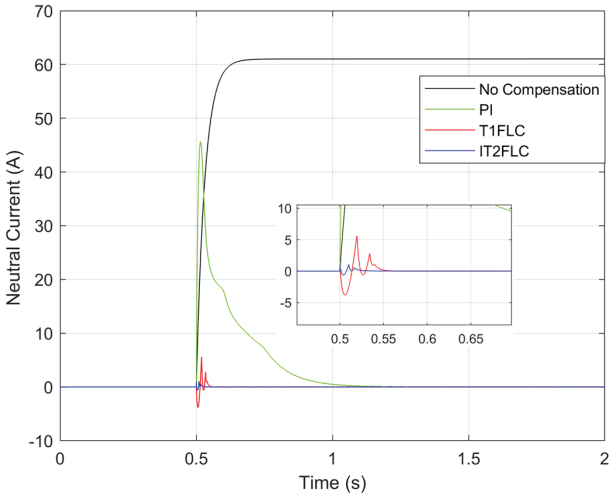

Fig. 18. Neutral current for positive 400V DC bias infused at 0.5s.

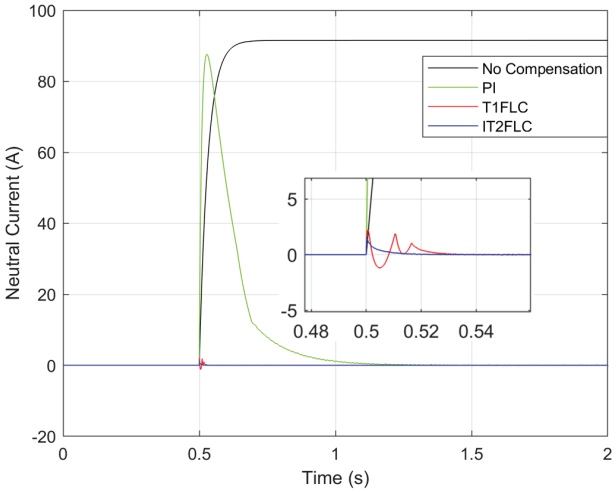

Fig. 19. Neutral current for positive 600V DC bias infused at 0.5s.

B. Scenario Two: Negative DC Bias

The simulation results of the three controllers under different negative direct current bias voltages are presented in this section. The boost converter was activated in the compensation device during these operations. Fig. 20, depicting the results for a -200V direct current bias voltage, shows that the PI control required 0.86 s to eliminate the bias and achieved a total settling time of 1.36 s. T1FLC eliminated the bias in 0.13 s, achieving

a settling time of 0.63 s, whereas IT2FLC removed the direct current bias in 0.08 s and had a settling time of 0.58 s.

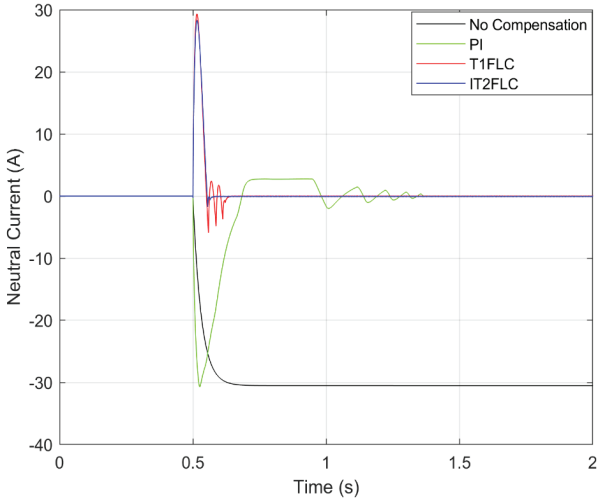

Fig. 20. Neutral current for negative 200V DC bias infused at 0.5s.

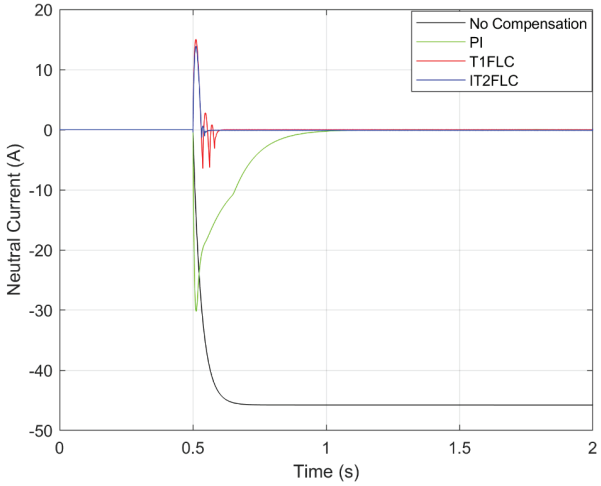

Fig. 21. Neutral current for negative 300V DC bias infused at 0.5s.

In the case of the -300V direct current bias voltage, Fig. 21 demonstrates that the PI control eliminated the bias in 0.51 s, achieving a settling time of 1.01 s. T1FLC removed the bias in 0.1 s, with a settling time of 0.6 s. IT2FLC, on the other hand, achieved direct current bias cancellation in just 0.06 s and had a settling time of 0.56 s. Furthermore, Fig. 22, showing the results for a -400V direct current bias voltage, shows that the PI control required 0.61 s to eliminate the bias and achieved a total settling time of 1.11 s. T1FLC eliminated the bias in 0.06 s, achieving a settling time of 0.56 s, whereas IT2FLC removed the direct current bias in 0.02 s and had a settling time of 0.02 s. Additionally, in the case of the -600V direct current bias voltage, Fig. 23 indicates that the PI control eliminated the bias in 0.69 s, achieving a settling time of 1.19 s. The bias was also eliminated with the use of T1FLC in 0.03 s, obtaining a settling time of 0.53 s, and IT2FLC eliminated the bias in 0.01 s while attaining a settling time of 0.51 s.

From these results, it can be inferred that the proposed IT2FLC outperformed T1FLC and PI controllers. It exhibited the smallest rise in current with no oscillations, in contrast to

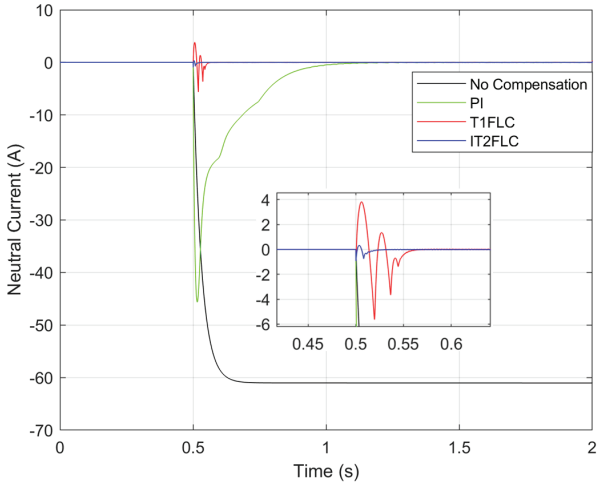

Fig. 22. Neutral current for negative 400V DC bias infused at 0.5s.

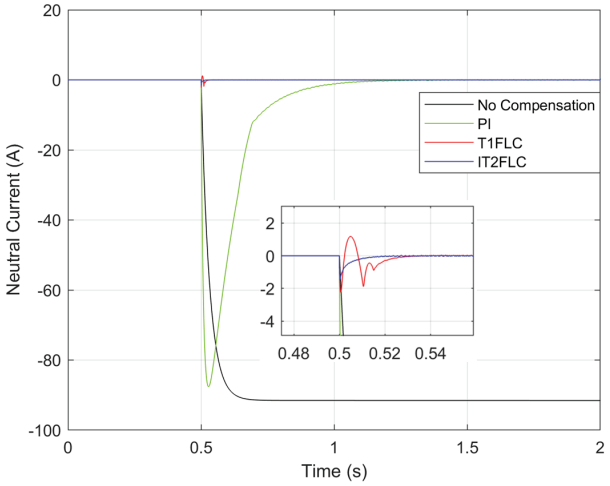

Fig. 23. Neutral current for negative 600V DC bias infused at 0.5s.

T1FLC. Additionally, it demonstrated a significantly enhanced transient response compared to both T1FLC and PI controls.

Table III shows a summary of all the results. Therefore, based on the results presented, it is evident that the dynamic performance of the proposed IT2FLC is highly robust and superior to that of the T1FLC and PI controls when managing the neutral direct current compensating system. Consequently, the IT2FLC proves to be a more effective choice for controlling the compensating device compared to the other controls.

TABLE III
DC BIAS RESULTS

		Negative DC Bias		Positive DC Bias	
		Transient Response (s)	Settling Time (s)	Transient Response (s)	Settling Time (s)
200V	PI	0.86	1.36	0.58	1.08
	T1FLC	0.13	0.63	0.21	0.71
	IT2FLC	0.08	0.58	0.07	0.57
300V	PI	0.51	1.01	0.54	1.04
	T1FLC	0.1	0.6	0.12	0.62
	IT2FLC	0.06	0.56	0.05	0.55
400V	PI	0.61	1.11	0.59	1.09
	T1FLC	0.06	0.56	0.05	0.55
	IT2FLC	0.02	0.52	0.03	0.53
600V	PI	0.69	1.19	0.64	1.14
	T1FLC	0.03	0.53	0.03	0.53
	IT2FLC	0.01	0.51	0.01	0.51

VI. Experimental Validation

Utilising a system comprising two three-phase core-type transformers, a bench-scale laboratory setup was conducted; the schematics is shown in Fig. 24. Apparatus involved 220/220 V, 300 VA three-phase transformer as the load transformer (transformer under test) and 400/400 V, 1 kVA three-phase transformer as source transformer, which was connected in back-to-back.

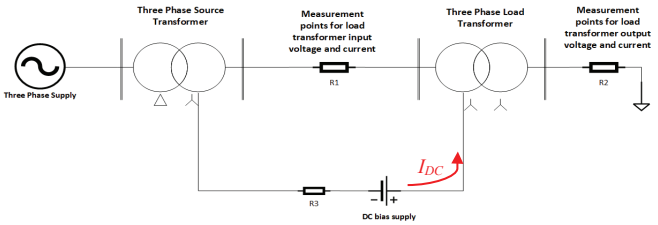

Fig. 24. Transformer under DC bias effects laboratory setup.

The source transformer provided power to the load transformer and was connected to a three-phase variable power source. As a source transformer, an isolation transformer was used to comply with the IEEE Std. 579-1992 convention and to ensure that DC bias was localised [29]. A 9 V battery was employed to generate very low DC bias injection levels into the transformer neutral, which was adjusted using a voltage divider to vary the quantity of DC bias injection. In addition, to ensure that the DC injection levels would not severely impact the magnetisation properties of the source transformer, the capacity of the source transformer was deliberately specified to be higher than the load transformer. The Picotech 25 MHz ±1400 V differential probe and PicoScope 6000 series were used to measure the current and voltage. The load transformer is the transformer under test. The hardware-implemented compensation device was incorporated into the setup, as shown in Fig. 2, at the load transformer neutral. Fig. 25 shows the setup of the rapid control prototype test. The buck-boost converter was implemented as the power module; this is shown in Fig. 26. The design specification and parameters of the components for the hardware implementation are shown in Table IV.

The control system manages the operation of the compensation device. Rapid Control Prototyping serves as the basis of the design structure for the control system by utilising a Speedgoat™ real-time system. The real-time system is made up of three parts: Speedgoat™ performance real-time target machine with an Intel 4.2 GHz core i7-7700K quad-core CPU, analog and digital I/O module (IO135) and an I/O318-100k reconfigurable FPGA module (Xilinx Spartan 6 100k) with a clock frequency of 75 MHz. MATLAB/Simulink® was used to create and evaluate the control algorithms in a simulation environment. The Simulink Real-Time™ and HDL Coder™ automatically generate the codes from the Simulink models and deploy them to the CPU and FPGA, respectively. Two analog input channels were used on the IO135 module: the first was for sensing the transformer neutral via a shunt resistor, and the second was for monitoring the output of the compensation device (power module). The two input channels were interfaced with the Simulink model on the CPU to generate the duty cycle required by the FPGA module. The FPGA module (IO318-100k) was configured to produce the PWM firing signals needed by the power module based on the DC bias voltage signal sensed at the transformer neutral, at a switching frequency of 50 kHz. This FPGA module was then used to interface the generated PWM signal with the MOSFET gate driver of the power module while the CPU real-time simulation ran at a sampling time of 50 µs.

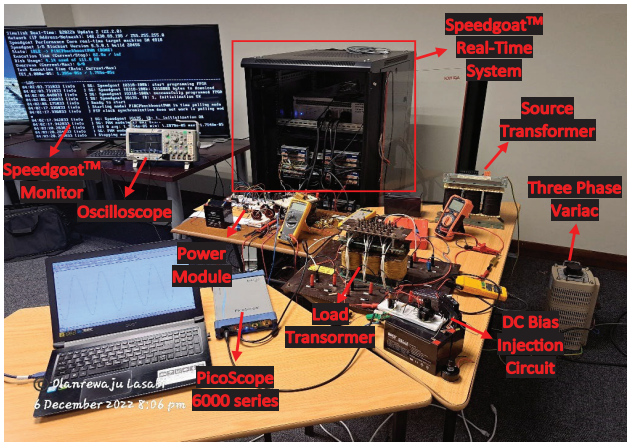

Fig. 25. Rapid control prototype test with the real-time system.

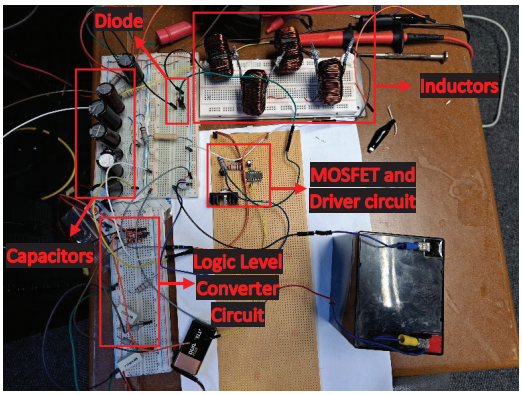

Fig. 26. Hardware implementation of the power module.

A. Experimental Results

The rapid control prototype test was implemented to verify the practicality of the proposed IT2FLC control function of the neutral DC compensation device. The results were obtained in real-time to validate the simulation results. Two levels of positive DC bias current (800 mA and 1.2 A) were injected into the transformer neutral in order to evaluate and compare the response of each type of controller in real-time. The transformer neutral current, the input signal to the control module of the compensation device, was measured via a shunt resistor. The output of the compensation device was monitored and measured as a reference to the neutral direct current to monitor the response of the compensation device to the presence of DC bias in the transformer neutral.

TABLE IV
Circuit Parameters for Hardware Implemented Power Module

DC-DC Converter	Inductance (µH)	Capacitance (µF)	Input Voltage (V)	Output Voltage (V)	Switching Frequency (kHz)
Buck-Boost	430	4600	12	100	50

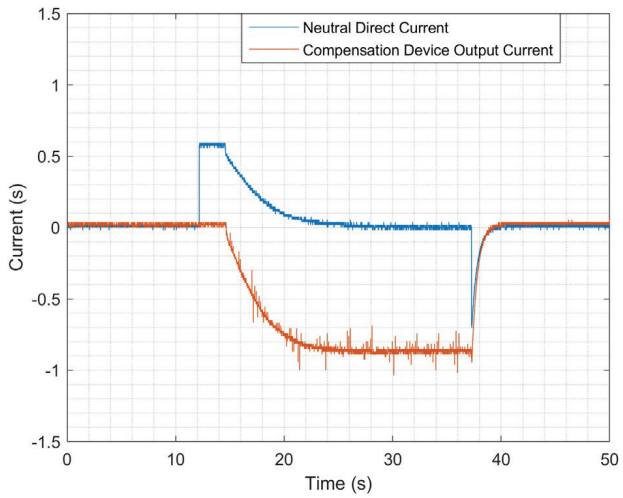

Fig. 27. DC bias (800 mA) mitigation with PI-based compensation device.

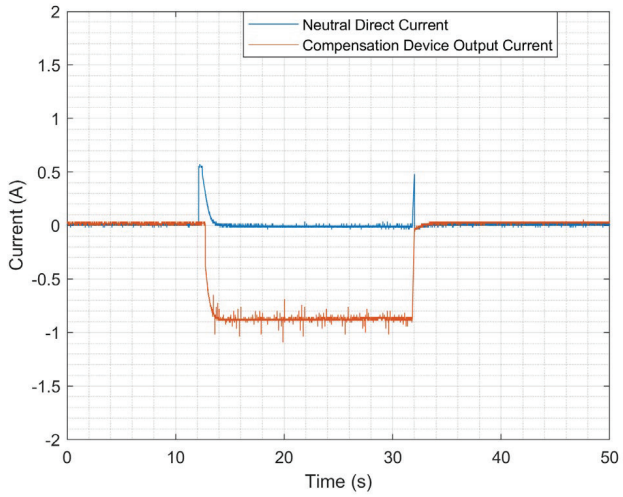

Fig. 28. DC bias (800 mA) mitigation with T1FLC-based compensation device.

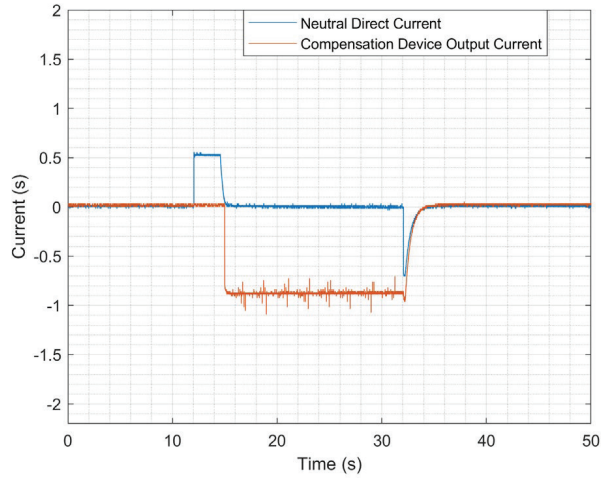

Fig. 29. DC bias (800 mA) mitigation with IT2FLC-based compensation device.

Fig. 27 presents the results obtained using the PI-based compensation device for mitigating DC bias. The 800 mA DC bias was injected at 12s. The conventional PI-based device started operating after 2.5s of DC bias injection but offset the DC bias within 11.5s, attaining zero steady-state error at 26s. The T1FLC-based compensation device started its operation after 2.9s of DC bias injection, as shown in Fig. 28, and attenuated the DC bias within 300ms, reaching zero steady-state error after 15.2s. In the case of the IT2FLC-based device, depicted in Fig. 29, its operation started after 700ms of DC bias injection and offset DC bias within a second, attaining zero steady-state error at 13.7s. In all three results, It can be observed that as soon as the DC bias was switched off, the neutral compensation device immediately stopped its current output and returned to its standby mode.

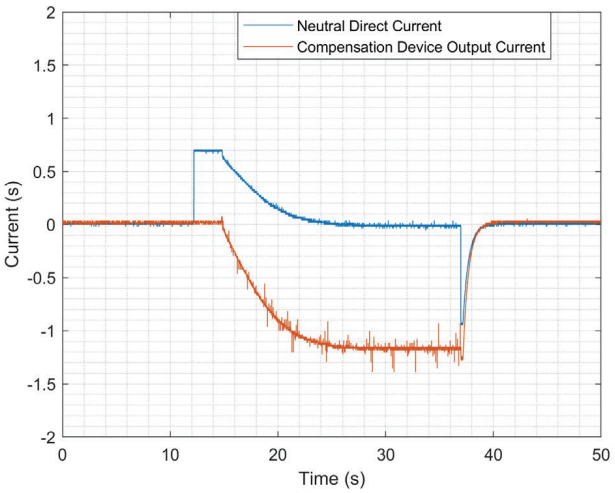

Fig. 30. Neutral DC bias (1.2 A) mitigation with PI-based compensation device.

The magnitude of the DC bias was varied by increasing to 1.2 A, and the test results obtained using the PI-based compensation device for mitigating DC bias are shown in Fig. 30. The PI-based device started after 2.8s of DC bias injection and off-set DC bias within 10.4s, reaching zero steady-state error at 25.2s. The T1FLC-based device, shown in Fig. 31, started operating after 3.8s of DC bias injection and attenuated DC bias within 600ms, attaining zero steady-state error at 16.4s. In the case of the IT2FLC-based device, depicted in Fig. 32, its operation started after 800ms of DC bias injection and offset DC bias within 700ms, attaining zero steady-state error at 13.5s. Among the three controllers used, it is evident that IT2FLC performed better, attaining zero steady-state error in the shortest possible time, coupled with an improved transient response compared to the PI-based and T1FLC-based compensation devices. The experimental results of the PI-based neutral compensation device are in line with the experimental results obtained by previous research [8], where the PI-based device mitigated the DC bias within 10s. It should be noted that the noise observed in the results of the current output for the compensation device can be attributed to the hardware implementation of the power module on a solderless breadboard and the jumper connecting wires. Breadboards possess small parasitic capacitors and inductors in the order of

pF and nH, respectively, creating oscillators (with large oscillation frequencies) with components.

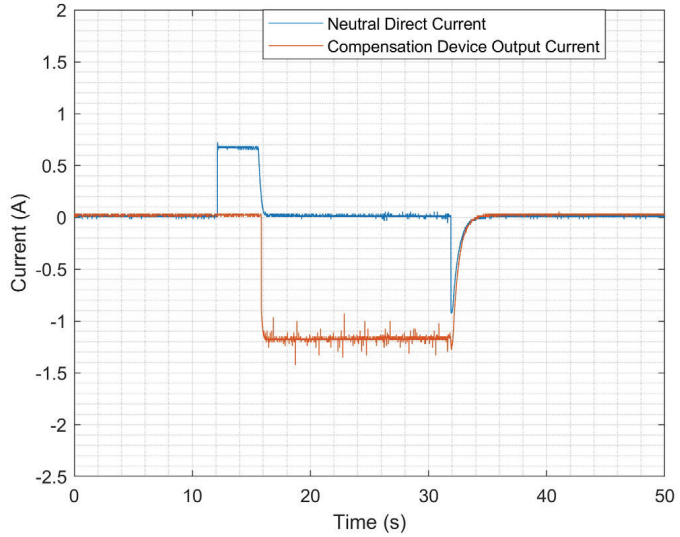

Fig. 31. DC bias (1.2 A) mitigation with T1FLC-based compensation device.

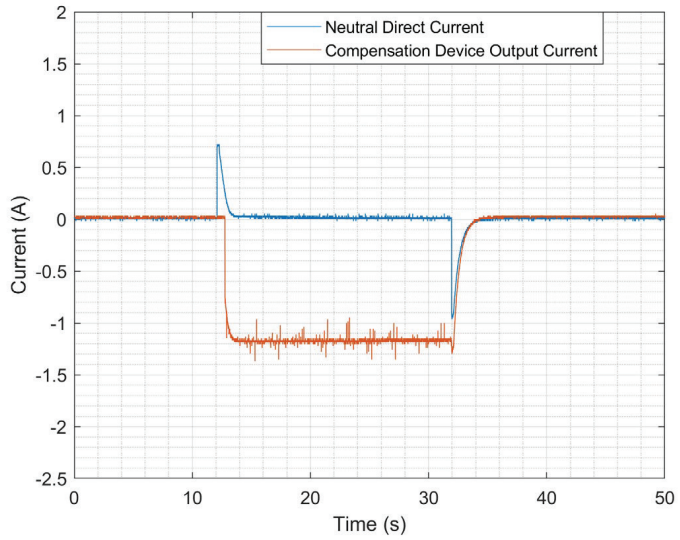

Fig. 32. DC bias (1.2 A) mitigation with IT2FLC-based compensation device.

The experimental results confirm and validate that the IT2FLC-based compensation device, performing better than the T1FLC and conventional PI-based, is more robust in controlling the device. In addition, the better performance of IT2FLC over T1FLC can be attributed to the increase in the number of parameters and degree of freedom possessed by IT2FLC, which makes it handle uncertainties more effectively and efficiently than T1FLC. The compensation device can eliminate DC bias, keeping the power transformer safe in its normal operating condition. This implies that the no-load noise and no-load losses are reduced and brought back to their normal minimal range. It also indicates a significant reduction in reactive power consumption. The test results also demonstrate that the control module of the neutral DC compensation device can avoid the excessive output current that may overload the device. The IT2FLC-controlled compensation device has also shown its effectiveness in various circumstances during the testing: when switching on or off the DC bias and its magnitude varied, the controller responded swiftly to prevent the transformer core from saturation.

VII. Conclusions

The neutral DC compensation method is an active approach for reducing DC bias in transformer neutrals by compensating the DC bias and restricting the direct MMF of transformer cores. This article presents the effects of DC bias on power transformers by analysing the exciting current of the transformer under DC bias voltage variations. A transformer-neutral DC compensating device featuring an innovative controller was proposed to tackle the issue. The compensating system, which consists of a power module and a novel control, was examined using both simulation models developed on MATLAB/Simulink® and a rapid control prototype testing using the Speedgoat™ performance real-time target machine. An interval type-II fuzzy logic control (IT2FLC) was proposed to control the compensation device. To determine the robustness of IT2FLC on the performance of the compensation device, the device was also controlled by utilising T1FLC and PI controllers. Transient response, oscillations, and settling time of the compensating device under varying DC bias voltages were considered as the performance criteria. Simulation results indicated that T1FLC performed better than the PI controller regarding performance criteria under different DC bias voltages considered. Compared with T1FLC, IT2FLC performed better in the control of the compensation device. This might be because IT2FLC can handle uncertainty in rules and parameters of the input MFs that occur in T1FLC; thus, IT2FLC is better suited for controlling the neutral DC compensation system compared to the other controls.

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